Direct RF Sampling Monopulse Receiver With Adaptive Phase And Power Calibration

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***Abstract*- Demand of compact and programmable system is leading to the development of receivers which can convert beam to bits as near as antennae to remove any intermediate down-convertor stage . Analog receivers are getting replaced by Direct RF sampling receivers which can perform the combine task of analog down convertor as well as IF sampling receivers. The paper discusses about the L-band Monopulse receivers which identify the target by comparing power in Sigma and Delta channel and estimates the angle of arrival by phase information. In this paper, direct RF sampling receiver is discussed which eliminates down convertor stage. The paper discusses about limitation of gain and phase matching in existing receivers and new method has been introduced which can calibrate receiver in terms of phase and power using digitally implemented algorithms rather than hardware so the error in estimation of angle of arrival of target can be minimized.**

***Keywords*-Monopulse, under-sampling, Direct RF sampling, digital calibration**

I. INTRODUCTION

Monopulse is a technique for accurate measurement of angle of arrival from a single reply pulse. Shortcomings of primary radar which are unable to distinguish one aircraft to another similar aircraft as well as height to sufficient accuracy is overcome by Secondary Surveillance Radar(SSR) [1]. SSR has an Interrogator(fitted with the main radar system or on airborne platform) and a transponder(fitted on target aircraft). SSR is widely used for target identification as a friend or foe, thereby also called as IFF(Identification Friend or Foe) [2]. The interrogator transmits pulsed signal in a particular mode of interrogation. Aircraft fitted with compatible transponder receives the interrogation signal and replies back in the form of another coded signal . These coded replies are received by the interrogator and processed for identification.

Monopulse receivers receive sum and delta inputs from antennae. Measurement of power in Sum and Delta channel gives the lateral displacement of target from the focal plane. The angle-error detector output is bipolar video whose polarity corresponds to the direction of error. If the power in both channel is same, then the target is at the axis. Any deviation in target from axis results into imbalance in power received by receiver in two channels. Because of this, gain matching within ±0.5dB and phase matching within ±5° is required.

In the existing analog receiver, among the sum and delta channel, phase and power is balanced by MMICs. The analog chips like phase shifter , variable attenuators are used to maintain two ideal channels as shown in Fig. 1. But in real time scenario, with the temperature variance or cable length mismatch , it becomes a difficult activity to maintain two ideal channels in system to system. Sigma output($\sum$) as well as delta output(Δ) is processed by IF sampling receiver which is a separate module. Direct RF sampling receiver discussed in this paper combine the feature of RF front-end receiver and IF sampling receiver which samples RF directly from antennae eliminating down-convertor stage. The receiver discussed in this paper combines the programmability of IF sampling receiver and performance of analog down-convertor.

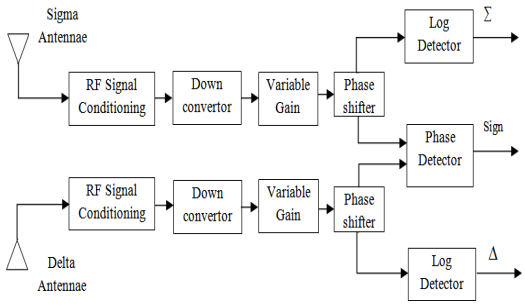

Figure 1. Existing analog receiver

II. SYSTEM DESCRIPTION

Programmability in receiver shown in Fig.1 can be included if analog blocks can be implemented digitally. Compact receiver can be realized by eliminating down convertor stage. Direct RF sampling receiver shown in Fig.1 includes above features . RF signal conditioning block used in Fig.1 is common to the receiver designed in Fig. 2. Remaining hardware blocks are replaced by programmable digital blocks reducing the hardware on board. Receiver shown in Fig. 2 ,along with the two channels ,Sigma and Delta, provision is provided to calibrate system through Cal signal.

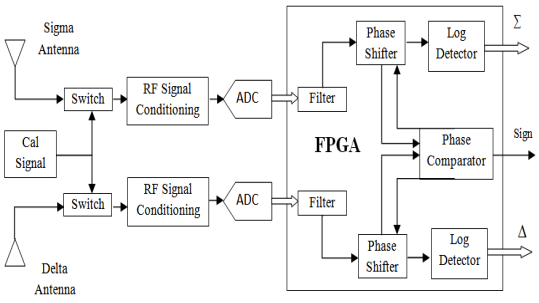

Figure 2. Direct RF Sampling Receiver

The selection of path i.e. real time target identification or calibration is through RF switch at the front end. Monopulse receiver specifies power matching within ±0.5 dB between two channels and phase matching between ±5º [3]. Digital receiver implemented can avoid the constraints for PCB design and can adapt the scenario with mismatched cable lengths also. Using the ASICs onboard to perform calibration increases the BOM as well as parameters which can vary over environment situation. The receiver implementing RF ASIC operation using signal processing algorithms can overcome this issue.

III. IMPLEMENTATION

Signal Conditioned RF is under-sampled . Under-sampling frequency depends on the bandwidth. According to Nyquist Shannon theorem , if under sampling frequency is selected twice the bandwidth , then it is ideal for sampling. But as the sampling frequency decreases, Nyquist zone narrows. Because of narrow Nyquist zone, unwanted frequencies get down converted near to wanted frequency which leads to the design of sharp band pass filter inside FPGA as well RF. To avoid this, under sampling frequency is selected by Eq. 1

$$\text{Fsample} = (4 \quad \text{IF})/(2\text{NZ} - 1) \tag{1}$$

where *Fsample* =sampling frequency
IF =carrier frequency
NZ =Nyquist zone

SNR of RF ADC depends on the jitter of sampling clock frequency (Fsample). Based on dynamic range required, processing bandwidth and minimum sampling frequency possible, clock source is chosen to meet SNR in Eq. 2

$$\text{SNR} = -20\log_{10}(2\pi f \text{jTotal}) \tag{2}$$

$$\text{jTotal} = \sqrt{\text{jADC}^2 + \text{jCLOCK}^2} \tag{3}$$

where:
jTotal = rms summation of clock and ADC aperture jitter
jADC =ADC internal aperture jitter
jCLOCK =rms jitter of the clock

Under-sampled data from both ADCs are processed by FPGA. Before real time identification , calibration among channel is required in terms of phase, gain and DC offset. The band pass filter implemented inside FPGA serves two function, one is to maintain programmable bandwidth as well as to remove any DC offset caused due to ADC[4]. In calibration, phase matching is followed by gain matching, Phase matching block consists of phase comparator and phase shifter. Phase comparator and phase shifter in digital domain is implemented using delay elements and Hilbert filter. To calculate phase, one of the path i.e. from sigma antenna(Sigma) or delta antenna(Delta) is passed through Hilbert filter. In the design, data coming from delta antenna is passed through 31 taps Hilbert filter. In phase and out of phase components are derived from multiplication of Sigma, Delta and Hilbert filter output(Hilb). Hilb is resultant from convolution of 31 taps Hilbert filter coefficients and Delta as

$$\text{Hilb} = \text{filter}(\text{Hcoeff}, 31, \text{Delta}) \tag{4}$$

$$i = \text{filter}(\text{Sigma}, \text{Hcoeff}) \tag{5}$$

$$q = \text{filter}(\text{Hilb}, \text{Hcoeff}) \tag{6}$$

Phase offset between Sigma and Delta is calculated from Eq. 5 and Eq. 6 as

$$\text{Phase} = \tan^{-1}(\text{filter}(q)/\text{filter}(i)) \tag{7}$$

Eq.7 gives phase comparison values of the resolution of 0.07 °. To reduce memory used in implementing lookup table, lookup table is designed from rounded off accuracy of 1°. Sign of *i* from Eq. 5 and sign of *q* from Eq. 6 gives the quadrant information which is required to know the which channel is leading or lagging[5]. To compensate the phase in lagging channel(Lag), phase shifter implemented in corresponding channel is activated. Phase shifting for a particular channel is implemented by splitting data captured i.e. Delta or Sigma into in-phase and out of phase component. Depending on the sign of *i* and *q*, they are multiplied with the split in-phase and out of phase component. Desired phase shift is obtained by Eq. 10.

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Phase adjustment is followed by gain adjustment. Gain adjustment block consists of log detector, digital attenuator and digital level comparator , all of them implemented inside FPGA. Phase adjusted samples are processed by log detector. Inside FPGA, log detectors are implemented by look up table of 0.5dB resolution. In calibration stage, instead of pulsed input CW Cal signal is used[6]. Output of log detector for CW signal is constant DC voltage corresponding to input power level. Digital level comparator compares the DC voltage difference which is having resolution of 0.5dB. Based on the difference and its sign , specified channel is attenuated by that value.

Once the channels are calibrated, a flag is generated to specify that calibration is over. This is followed by real time target identification which included pulse demodulation for Sigma as well as delta channel and phase sign .

IV. Test Results

Pulse modulated RF input is fed to both channels whose pulse width is 0.45 us. Data is capture on High end Tektronix CRO shown in Fig. 3

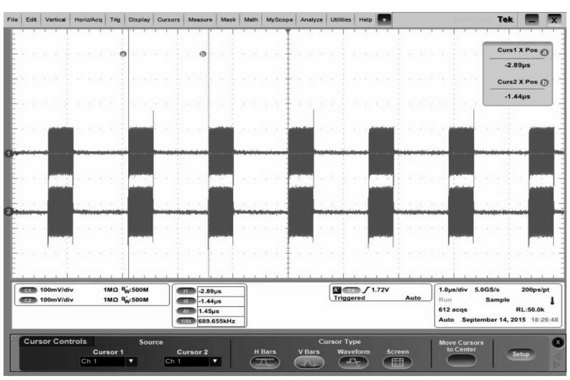

Figure 3. Dual channel pulse modulated input to receiver

Fig.4 shows the calibration of receiver where the first two waveform shows the data captured by RF ADCs, next two waveform shows the filtered data . The phase difference between is calculated as 62°. The next two waveform shows the phase matched signals.

Figure 4. Output of phase shifter

Fig. 5 shows the calibrated input in terms of phase and gain.

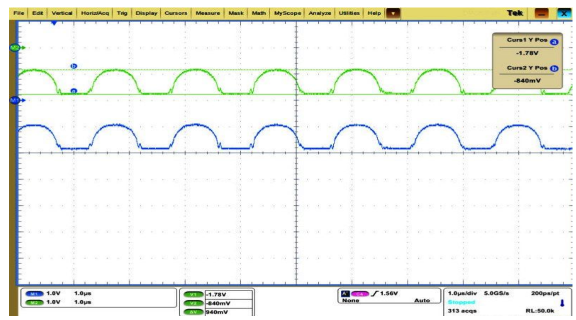

Figure 5. Phase as well gain matched output

Fig. 6 shows the output of Monopulse receiver i.e. demodulated pulse as well as sign bit. Sign bit is generated when the phase difference between the channels cross 90°.

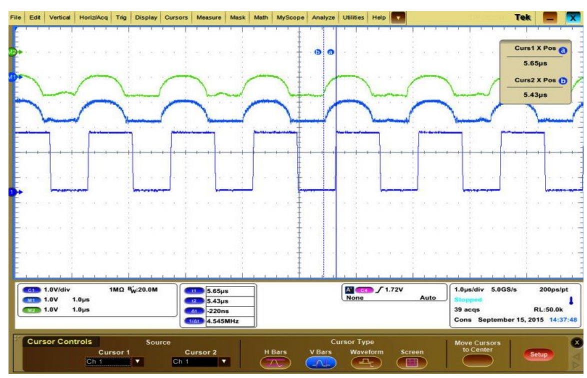

Figure 6. Output of Monopulse receiver

V. CONCLUSION

Direct RF sampling receiver provides much flexibility on receiver compared to analog receiver. The digitally implemented phase as well as gain calibration algorithm reduces the effort to be put in PCB design. The algorithm is suitable to be used for different RADAR application.

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Vikas Kumar-Obtained his B.E from UVCE Bangalore in 2012.He joined BEL in 2012 and since then he is working in RF group as Deputy Engineer. He has worked on L-Band transmitter and receivers, Signal processing for proximity sensor , controller for radio relays and synthesizers and Signal processing for Digital Receiver.

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Kalyani Murthy – Kalyani Murthy joined BEL in 1985 at Tactical Communications group after graduating in Electronics & Communications Engineering from BIT, Ranchi University. She has worked on HF & VHF Man pack and handheld Radio systems and associated Frequency synthesizer subsystems. Moved to Core RF design group in 2000 and involved in design of various RF Trans-receiver modules and Frequency sources for Communications and Radar systems. Worked at Corporate Strategic Planning division from 2007-12. Currently heading the RF components (RFC) group of Central D&E since 2012.